

What is claimed is:

- 1 1. A temperature detecting circuit comprising:
2 a first, second and third voltage divider, each of
3 which comprises resistors having temperature-
4 dependent resistances, outputting a first, second
5 and third voltage; and
6 a voltage comparator comparing the first voltage with
7 the second voltage, and the first voltage with
8 the third voltage and respectively outputting a
9 first and second signal according to the
10 comparison results.
- 1 2. The circuit as in claim 1, wherein the voltage
2 comparator comprises:
3 a first transistor of a first type having a source
4 coupled to receive a first voltage;
5 a second transistor of the first type having a gate
6 coupled to a gate of the first transistor, a
7 source coupled to receive the first voltage and a
8 drain outputting a first bit of a temperature
9 detection signal;
10 a third transistor of the first type having a gate
11 coupled to the gate of the first transistor, a
12 source coupled to receive the first voltage and a
13 drain outputting a second bit of the temperature
14 detection signal;
15 a fourth transistor of a second type having a drain
16 coupled to a drain of the first transistor;

17 a fifth transistor of the second type having a drain
18 coupled to the drain of the second transistor and
19 a source coupled to a source of the fourth
20 transistor;
21 a sixth transistor of the second type having a drain
22 coupled to the drain of the third transistor and
23 a source coupled to the source of the fourth
24 transistor; and
25 a seventh transistor of the second type having a drain
26 coupled to the drain of the fourth transistor, a
27 gate coupled to receive an enable signal and a
28 source coupled to receive a second voltage.

1 3. The circuit as in claim 2, wherein the voltage
2 divider comprises:
3 a first resistor coupled between the gate of the fourth
4 transistor and the source of the first
5 transistor;
6 a second resistor coupled between the gate of the
7 fourth transistor and the source of the seventh
8 transistor;
9 a third resistor coupled between the gate of the fifth
10 transistor and the source of the first
11 transistor;
12 a fourth resistor coupled between the gate of the fifth
13 transistor and the source of the seventh
14 transistor;
15 a fifth resistor coupled between the gate of the sixth
16 transistor and the source of the first
17 transistor; and

18 a sixth resistor coupled between the gate of the sixth
19 transistor and the source of the seventh
20 transistor.

1 4. The circuit as in claim 2, wherein the first and
2 second types are P and N type, respectively.

1 5. The circuit as in claim 2, wherein the first and
2 second voltages are Vdd and a ground voltage, respectively.

1 6. The circuit as in claim 3, wherein the first,
2 fourth, fifth and sixth resistors are made of poly-silicon.

1 7. The circuit as in claim 3, wherein the second and
2 third resistors are parasitic resistances of an N well.

1 8. A circuit for controlling a self-refresh period of
2 a semiconductor memory device, comprising:
3 a pulse generating circuit which outputs a periodic
4 pulse train in response to an external control
5 signal;
6 a frequency-dividing circuit which outputs a plurality
7 of pulse trains having different periods from
8 each other by frequency-dividing said periodic
9 pulse train output by said pulse generating
10 circuit;
11 a temperature detecting circuit which detects an
12 ambient temperature of said memory device and
13 outputs a temperature detection signal when said
14 ambient temperature reaches a predetermined
15 temperature level, the temperature detection
16 circuit comprising:

17 a first transistor of a first type having a source
18 coupled to receive a first voltage;
19 a second transistor of the first type having a
20 gate coupled to a gate of the first
21 transistor, a source coupled to receive the
22 first voltage and a drain outputting a first
23 bit of the temperature detection signal;
24 a third transistor of the first type having a gate
25 coupled to the gate of the first transistor,
26 a source coupled to receive the first
27 voltage and a drain outputting a second bit
28 of the temperature detection signal;
29 a fourth transistor of a second type having a
30 drain coupled to a drain of the first
31 transistor;
32 a fifth transistor of the second type having a
33 drain coupled to the drain of the second
34 transistor and a source coupled to a source
35 of the fourth transistor;
36 a sixth transistor of the second type having a
37 drain coupled to the drain of the third
38 transistor and a source coupled to the
39 source of the fourth transistor;
40 a seventh transistor of the second type having a
41 drain coupled to the drain of the fourth
42 transistor, a gate coupled to receive an
43 enable signal and a source coupled to
44 receive a second voltage; and
45 six resistors respectively coupled between the
46 gate of the fourth transistor and the source

47 of the first transistor, the gate of the
48 fourth transistor and the source of the
49 seventh transistor, the gate of the fifth
50 transistor and the source of the first
51 transistor, the gate of the fifth transistor
52 and the source of the seventh transistor,
53 the gate of the sixth transistor and the
54 source of the first transistor, the gate of
55 the sixth transistor and the source of the
56 seventh transistor;

57 a voltage detection circuit which detects a power
58 supply voltage applied to said memory device and
59 outputs a voltage detection signal when said
60 power supply voltage reaches a predetermined
61 voltage level; and,

62 a pulse selection circuit which outputs a self-refresh
63 master clock by selecting one of said pulse
64 trains in response to said temperature detection
65 signal and said voltage detection signal.

1 9. The circuit as in claim 8, wherein the first and
2 second type are P and N type, respectively.

1 10. The circuit as in claim 8, wherein the first and
2 second voltages are Vdd and a ground voltage, respectively.

1 11. The circuit as in claim 8, wherein the first,
2 fourth, fifth and sixth resistors are made of poly-silicon.

1 12. The circuit as in claim 8, wherein the second and
2 third resistors are parasitic resistances of an N well.

1 13. A circuit for controlling a self-refresh period of
2 a semiconductor memory device, comprising:
3 temperature detecting circuit outputting a temperature
4 detection signal, comprising:
5 a first transistor of a first type having a source
6 coupled to receive a first voltage;
7 a second transistor of the first type having a
8 gate coupled to a gate of the first
9 transistor, a source coupled to receive the
10 first voltage and a drain outputting a first
11 bit of the temperature detection signal;
12 a third transistor of the first type having a gate
13 coupled to the gate of the first transistor,
14 a source coupled to receive the first
15 voltage and a drain outputting a second bit
16 of the temperature detection signal;
17 a fourth transistor of a second type having a
18 drain coupled to a drain of the first
19 transistor;
20 a fifth transistor of the second type having a
21 drain coupled to the drain of the second
22 transistor and a source coupled to a source
23 of the fourth transistor;
24 a sixth transistor of the second type having a
25 drain coupled to the drain of the third
26 transistor and a source coupled to the
27 source of the fourth transistor;
28 a seventh transistor of the second type having a
29 drain coupled to the drain of the fourth

30 transistor, a gate coupled to receive an
31 enable signal and a source coupled to
32 receive a second voltage; and
33 six resistors, with each resistor respectively
34 coupled between the gate of the fourth
35 transistor and the source of the first
36 transistor, the gate of the fourth
37 transistor and the source of the seventh
38 transistor, the gate of the fifth transistor
39 and the source of the first transistor, the
40 gate of the fifth transistor and the source
41 of the seventh transistor, the gate of the
42 sixth transistor and the source of the first
43 transistor, the gate of the sixth transistor
44 and the source of the seventh transistor;
45 an internal period selector receiving a plurality of
46 signals representing different periods and
47 outputting one of the signals according to the
48 temperature detection signal from the temperature
49 detecting circuit;
50 a plurality of timers, each generating one of the
51 signals representing the different periods; and
52 a self-refresh controller determining a refresh period
53 according to the signal output from the internal
54 period selector.

1 14. The circuit as in claim 13, wherein the first and
2 second type are P and N type, respectively.

1 15. The circuit as in claim 13, wherein the first and
2 second voltages are Vdd and a ground voltage, respectively.

1 16. The circuit as in claim 13, wherein the first,
2 fourth, fifth and sixth resistors are made of poly-silicon.

1 17. The circuit as in claim 13, wherein the second and
2 third resistors are parasitic resistances of an N well.